2026 1st International Electronics & Packaging Technology Conference

BRIDGING SKILLS & INNOVATION FOR INDIA'S INDUSTRY (EPTC INDIA)

IEEE EPT Conference 206 is an international conference organized by the IEEE EPS Delhi Chapter and co-sponsored by the IEEE Electronics Packaging Society (EPS) along with Manav Rachna International Institute of Research & Studies on March 2nd - 3rd, 2026.

Set in the backdrop of a verdant, green campus in the Aravalli hills, the event is hosted at Manav Rachana International Institute of Research & Studies, Faridabad, Delhi-NCR. It will feature keynotes, tutorials, technical sessions, invited talks, panels, workshops, exhibitions, and networking activities.

Topics include modules, components, materials, equipment technology, assembly, reliability, interconnect design, device and systems packaging, heterogeneous integration, wafer-level packaging, flexible electronics, LED, IoT, 5G, emerging technologies, 2.5D/3D integration technology, smart manufacturing, automation, and AI. Planned in tandem with the Gujarat Semiconnect, the event is expected to pull in ~250 academia/industry participants.

Theme Sessions:

Executed with keynotes and technology talks from an eclectic group of distinguished speakers from IEEE, Industry, Government and academic stakeholders, the session will cover the following tracks covering emerging trends, technologies, and challenges in electronics packaging:

1. Advanced Packaging Technologies
- Heterogeneous Integration and System-in-Package (SiP)
- Fan-Out Wafer-Level Packaging (FOWLP)
- 3D IC and Through-Silicon Vias (TSVs)
- Advanced Substrates and Interposers

2. Materials and Processes for Packaging
- Advanced Materials for High-Performance Packaging
- Thermal Interface Materials (TIMs) and Management
- Soldering, Adhesives, and Encapsulation Materials
- Additive Manufacturing and 3D Printing for Packaging

3. Reliability and Testing
- Failure Analysis and Reliability Testing
- Mechanical and Thermal Stress Testing
- Advanced Metrology for Packaging
- Predictive Maintenance and AI-Driven Reliability Models

4. Power and RF Packaging
- Power Electronics Packaging and Thermal Management
- Packaging for High-Frequency and RF Applications
- Wide Bandgap Semiconductors (SiC, GaN) Packaging
- Electromagnetic Interference (EMI) Shielding

5. Emerging Applications
- Packaging for IoT and Wearable Devices
- Packaging for Quantum Computing
- Automotive and Aerospace Packaging
- Biocompatible and Medical Device Packaging

6. Sustainable and Green Packaging
- Eco-Friendly Materials and Processes
- Recyclability and Circular Economy in Electronics Packaging
- Low-Carbon Manufacturing Techniques
- Lifecycle Assessment for Packaging Solutions

7. Advanced Interconnects and Integration
- High-Density Interconnects
- Flexible and Stretchable Electronics
- Optical Interconnects and Photonic Integration
- Wireless Interconnects and Antenna Integration

8. **Thermal and Mechanical Challenges**
- Heat Dissipation in High-Density Packaging
- Modeling and Simulation of Thermal and Mechanical Stress
- Thermal Interface Materials for Next-Gen Devices
- High-Performance Cooling Solutions

9. AI, ML, and Digital Twin in Packaging
- AI-Driven Design and Optimization
- Machine Learning for Predictive Analysis
- Digital Twins for Packaging Design and Testing
- Automation and Robotics in Packaging

10. Industry Trends and Standards
- Standardization in Packaging Processes and Materials
- Collaboration Across Academia and Industry
- Future Trends in Semiconductor Packaging
- Case Studies of Industry Innovation

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Tutorials:

With a focus on capacity building for AICTE/ESSCI approved curriculum for semiconductor design & manufacturing, a number of SME led tutorials are planned across the conference days for faculty development as well as industry and student engagement.

Manufacturing skills workshops: (in compliance with AICTE curriculum/ MSDE approved national occupation standards)

1. Industrial Safety for Semiconductors
2. Vacuum Technology for Semiconductors
3. OSAT Manufacturing Process Flow & Wafer Dicing
4. Cleanroom Technologies/Ultra Pure Water Technologies

Design Skills Workshops: (in compliance with ISM/MEITY and AICTE curriculum/ MSDE approved national occupation standards)

1. Learning Semiconductor Manufacturing process Flow with LAM Semulator 3D
2. Altium PCB Design and Manufacturing Workshop

Conference Venue:

Manav Rachana International Institute of Research & Studies, Sector 43, Aravalli Hills, Delhi-Surajkund Road, Faridabad, Haryana, Pin Code: 121004.

Important Dates:

Full Manuscript Submission Deadline	1st December 2025
Portal Opens	15th July 2025

Do not miss this opportunity to be part of International EPTC 2026 Delhi-NCR!
Please visit the conference website https://www.eptc.in/ for more information and updates.
Contact Details: +91-8800229768

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